IN THE CLAIMS:

Claims 3 and 21 have been amended and claims 29 through 32 have been added herein. Please note that pursuant to 37 C.F.R. § 1.121(c)(3), all claims currently pending and under consideration in the referenced application are shown below, in clean form, for clarity. Also attached, in accordance with 37 C.F.R. § 1.121(c)(1)(ii), is a version of the amended claims with markings to show changes made thereto.

Please enter these claims as amended.

1. (Previously Five Times Amended) A contact for a semiconductor device, comprising:

a single contact plug extending through a first barrier layer planarized down to a transistor gate member, said single contact plug in electrical communication with an active region on a semiconductor substrate;

an individual contact land disposed atop said single contact plug and a portion of said first barrier layer, wherein said contact land is wider than said single contact plug and is substantially planar;

an upper contact extending through a second barrier layer, said second barrier layer disposed over said first barrier layer, to form an electrical contact with said individual contact land.

3. (Six Times Amended) A transistor for the dissipation of electrostatic discharges, comprising:

an intermediate structure comprising a substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, said intermediate structure further including at least one transistor gate member spanned between said at least one implanted drain region and said at least one implanted source region on said at least one active area;

a first barrier layer planarized down to said at least one transistor gate member and substantially covering said at least one thick field oxide area, said at least one active area, and adjacent said at least one transistor gate member;

at least one drain contact plug extending through said first barrier layer, wherein said at least one drain contact plug is in electrical communication with said at least one drain region on said semiconductor substrate;

at least one source contact plug extending through said first barrier layer, wherein said at least one source contact plug is in electrical communication with said at least one source region on said semiconductor substrate;

an individual drain contact land disposed atop each of said at least one drain contact plugs and a portion of said first barrier layer, said individual drain contact land wider than said at least one drain contact plug and substantially planar;

an individual source contact land disposed atop each of said at least one source contact plugs and a portion of said first barrier layer, said individual source contact land wider than said at least one source contact plug and substantially planar;

a second barrier layer disposed over said first barrier layer, said individual drain contact land, and said individual source contact land;

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at least one upper source contact extending through said second barrier layer, said at least one upper source contact in electrical communication with at least one of said individual source contact lands; and

at least one upper drain contact extending through said second barrier layer, said at least one upper drain contact in electrical communication with at least one of said individual drain contact lands.

4. (Previously Amended) The transistor of claim 3, further comprising drain contact metallization in electrical communication with said at least one upper drain contact; and source contact metallization in electrical communication with said at least one upper source contact.

5. (Previously Twice Amended) The transistor of claim 3, wherein said at least one source contact plug extends between at least two source regions.

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6. (Previously Twice Amended) The transistor of claim 3, wherein said at least one drain contact plug extends between at least two drain regions.

9. (Previously Three Times Amended) The transistor of claim 3, wherein said at least one upper source contact extends between at least two individual source contact lands.

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10. (Previously Three Times Amended) The transistor of claim 3, wherein said at least one upper drain contact extends between at least two individual drain contact lands.

19. (Previously Five Times Amended) A semiconductor device including at least one contact, comprising:

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a single contact plug extending through a first barrier layer planarized down to a transistor gate member, said single contact plug in electrical communication with an active region on a semiconductor substrate;

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an individual contact land disposed atop said single contact plug and a portion of said first barrier layer, said individual contact land wider than said single contact plug and substantially planar; and

an upper contact extending through a second barrier layer, said second barrier layer disposed over said first barrier layer, to form an electrical contact with said individual contact land.

21. (Six Times Amended) A semiconductor device including at least one transistor for the dissipation of electrostatic discharges, comprising:

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an intermediate structure comprising a semiconductor substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, said intermediate structure further including at least one transistor gate member spanned between said at least one implanted drain region and said at least one implanted source region on said at least one active area;

a first barrier layer planarized down to said at least one transistor gate member and substantially covering said at least one thick field oxide area, said at least one active area, and adjacent said at least one transistor gate member;

at least one drain contact plug extending through said first barrier layer, wherein said at least one drain contact plug is in electrical communication with said at least one implanted drain region on said semiconductor substrate;

at least one source contact plug extending through said first barrier layer, wherein said at least one source contact plug is in electrical communication with said at least one implanted source region on said semiconductor substrate;

an individual drain contact land disposed atop said at least one drain contact plug and a portion of said first barrier layer, said individual drain contact land wider than said at least one drain contact plug and substantially planar;

an individual source contact land disposed atop said at least one source contact plug and a portion of said first barrier layer, said individual source contact land wider than said at least one source contact plug and substantially planar;

a second barrier layer disposed over said first barrier layer;

at least one upper source contact extending through said second barrier layer, said at least one upper source contact in electrical communication with at least one said individual source contact land; and

at least one upper drain contact extending through said second barrier layer, said at least one upper drain contact in electrical communication with at least one said individual drain contact land.

22. The semiconductor device of claim 21, further comprising drain contact metallization in electrical communication with said at least one upper drain contact; and source contact metallization in electrical communication with said at least one upper source contact.

23. (Previously Amended) The semiconductor device of claim 21, wherein said at least one source contact plug extends between at least two source regions.

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24. (Previously Amended) The semiconductor device of claim 21, wherein said at least one drain contact plug extends between at least two drain regions.

27. (Previously Amended) The semiconductor device of claim 21, wherein said at least one upper source contact extends between at least two individual source contact lands.

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28. (Previously Twice Amended) The semiconductor device of claim 21, wherein said at least one upper drain contact extends between at least two individual drain contact lands.

29. (New) A contact for a semiconductor device, comprising:

a single contact plug extending through a first barrier layer and a second barrier layer, said second barrier layer disposed over said first barrier layer and planarized down to a transistor gate member, said single contact plug being in electrical communication with an active region on a semiconductor substrate;

an individual contact land disposed atop said single contact plug and a portion of said second barrier layer, wherein said individual contact land is wider than said single contact plug;

an upper contact extending through a third barrier layer, said third barrier layer disposed over said second barrier layer, to form an electrical contact with said individual contact land.

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30. (New) A transistor for the dissipation of electrostatic discharges, comprising:

an intermediate structure comprising a substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, said intermediate structure further including at least one transistor gate member spanned between said at least one implanted drain region and said at least one implanted source region on said at least one active area;

a first barrier layer substantially covering said at least one thick field oxide area and said at least one active area, and adjacent said at least one transistor gate member;

a second barrier layer disposed over said first barrier layer and planarized down to said at least one transistor gate member;

at least one drain contact plug extending through each of said first and second barrier layers, wherein said at least one drain contact plug is in electrical communication with said at least one drain region on said semiconductor substrate;

at least one source contact plug extending through each of said first and second barrier layers, wherein said at least one source contact plug is in electrical communication with said at least one source region on said semiconductor substrate;

an individual drain contact land disposed atop each of said at least one drain contact plugs and a portion of said second barrier layer, said individual drain contact land wider than said at least one drain contact plug;

an individual source contact land disposed atop each of said at least one source contact plugs and a portion of said second barrier layer, said individual source contact land wider than said at least one source contact plug;

a third barrier layer disposed over said second barrier layer, said individual drain contact land, and said individual source contact land;

at least one upper source contact extending through said third barrier layer, said at least one upper source contact in electrical communication with said individual source contact land; and

at least one upper drain contact extending through said third barrier layer, said at least one upper drain contact in electrical communication with said individual drain contact land.

31. (New) A semiconductor device including at least one contact, comprising:

a single contact plug extending through each of a first barrier layer and a second barrier layer, said second barrier disposed over said first barrier layer and planarized down to a transistor gate member, said single contact plug being in electrical communication with an active region on a semiconductor substrate;

an individual contact land disposed atop said single contact plug and a portion of said second barrier layer, said individual contact land being wider than said single contact plug; and

an upper contact extending through a third barrier layer, said third barrier layer disposed over said second barrier layer, to form an electrical contact with said individual contact land.

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32. (New) A semiconductor device including at least one transistor for the dissipation of electrostatic discharges, comprising:

an intermediate structure comprising a semiconductor substrate having at least one thick field oxide area, and at least one active area including at least one implanted drain region, and at least one implanted source region, said intermediate structure further including at least one transistor gate member spanned between said at least one implanted drain region and said at least one implanted source region on said at least one active area;

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a first barrier layer substantially covering said at least one thick field oxide area and said at least one active area, and adjacent said at least one transistor gate member;

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a second barrier layer disposed over said first barrier layer and planarized down to said at least one transistor gate member;

at least one drain contact plug extending through each of said first and second barrier layers, wherein said at least one drain contact plug is in electrical communication with said at least one implanted drain region on said semiconductor substrate;

at least one source contact plug extending through each of said first and second barrier layers, wherein said at least one source contact plug is in electrical communication with said at least one implanted source region on said semiconductor substrate;

an individual drain contact land disposed atop said at least one drain contact plug and a portion of said second barrier layer, said individual drain contact land being wider than said at least one drain contact plug;

an individual source contact land disposed atop said at least one source contact plug and a portion of said second barrier layer, said individual source contact land being wider than said at least one source contact plug;

a third barrier layer disposed over said second barrier layer, said individual source contact land and said individual drain contact land;

at least one upper source contact extending through said third barrier layer, said at least one upper source contact being in electrical communication with said individual source contact land; and

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at least one upper drain contact extending through said third barrier layer, said at least one upper drain contact being in electrical communication with said individual drain contact land.